Bias Control Option Application Note

Reference: AN001

Oxidation Nanolithography using the Bias Control Option of the NSCRIPTOR™ DPN® System

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Introduction

The NSCRIPTOR™ DPN® System is a dedicated nanolithography tool developed by NanoInk. It produces nanoscale structures on a surface through the use of a single scanned probe tip or with an array of multiple tips. The NSCRIPTOR is optimized for the Dip Pen Nanolithography® (DPN) process. This process allows "ink" material to be directly deposited from a sharp pen tip onto a substrate with nanometer resolution and accuracy. In addition to doing DPN, this technology note shows that the NSCRIPTOR can be used for performing more general oxidation nanolithography without a coated tip.

The ability to create an electric field at the tip with respect to the sample, and to have a current flowing through the tip-sample junction, opens another dimension to the versatility of the NSCRIPTOR System. For example, DPN methods can be favorably combined with bias control, which was recently used to deposit several metals and semiconductors, on silicon, at room temperature.[1] Other powerful nanolithography techniques that are enabled with voltage bias control include electrostatic nanolithography in polymers[2] and oxidation nanolithography of thin metal films[3] or semiconductor samples.[4] These experiments can be done in contact mode as well as in AC mode.[5] Careful integration of the Bias Control Option with InkCAD™ software (the NSCRIPTOR user interface) provides user friendly control over the amount of voltage bias and the timing of the voltage signals during patterning.

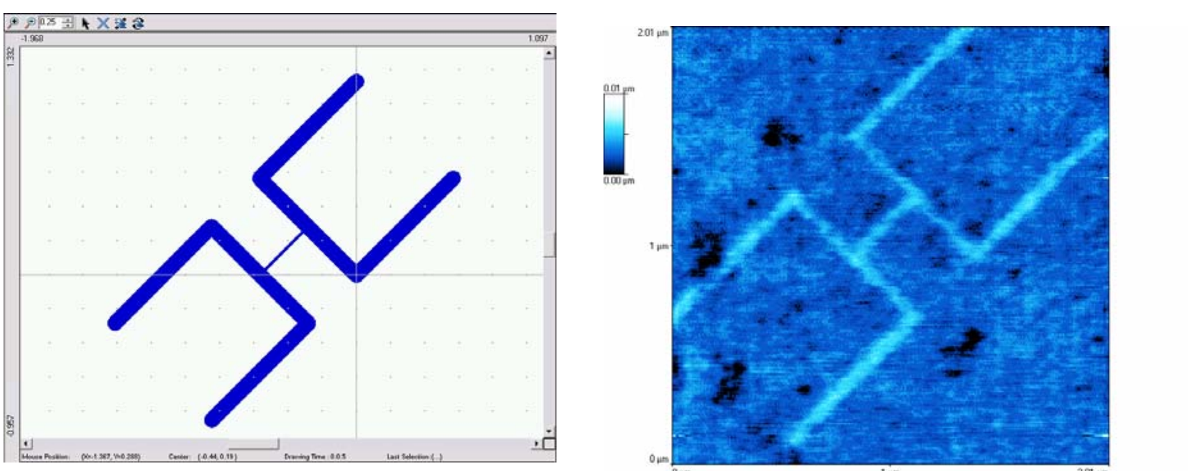

Figure 1: Design (left) and oxidization nanolithography structure (right); 2 µm scan size

As a case study in using a biased probe tip with NanoInk technology, we used tip-induced anodic surface oxidation of silicon, the most basic and straight-forward system. Here, a negative bias on the tip is used to locally oxidize a piece of cleaned silicon wafer. In this process, silicon dioxide is grown onto the silicon, and is then imaged using contact topography and lateral force imaging with the same probe that lithographically produced the oxidation pattern.

As a first step, an *n*-doped silicon wafer is cleaved into small pieces. To reduce specks and other surface contamination caused by cleaving, we first cleaned the samples in an ultrasonic bath of deionized water for 10 minutes, followed by 8 minutes of plasma cleaning in an argon atmosphere. Finally, buffered HF was used to strip the wafer of its native oxide. We found that the oxidation performance decreases within a few hours after cleaning, due to the thin native oxide that naturally grows on silicon under atmospheric conditions. Thus, we evaluated oxide removal by measuring contact resistance between two needle electrodes and the substrate. For lithography, we used three different probe types, and found them all to work. The probe types tested were Veeco Ultralever™ silicon probes, NT-MDT Ultrasharp™ silicon probes and NanoWorld™ platinum-coated silicon probes. HF-cleaned probes showed no performance improvement over unclean ones.

As an example, we designed and patterned a structure that could be used as an electron tunnel barrier for nanoelectronic applications. Figure 1 shows the design window in InkCAD and the resulting structure using a positive bias of 10V on the sample (i.e., the tip had a relative negative bias). Humidity was set to 20% and the write speed was 1 µm/sec.

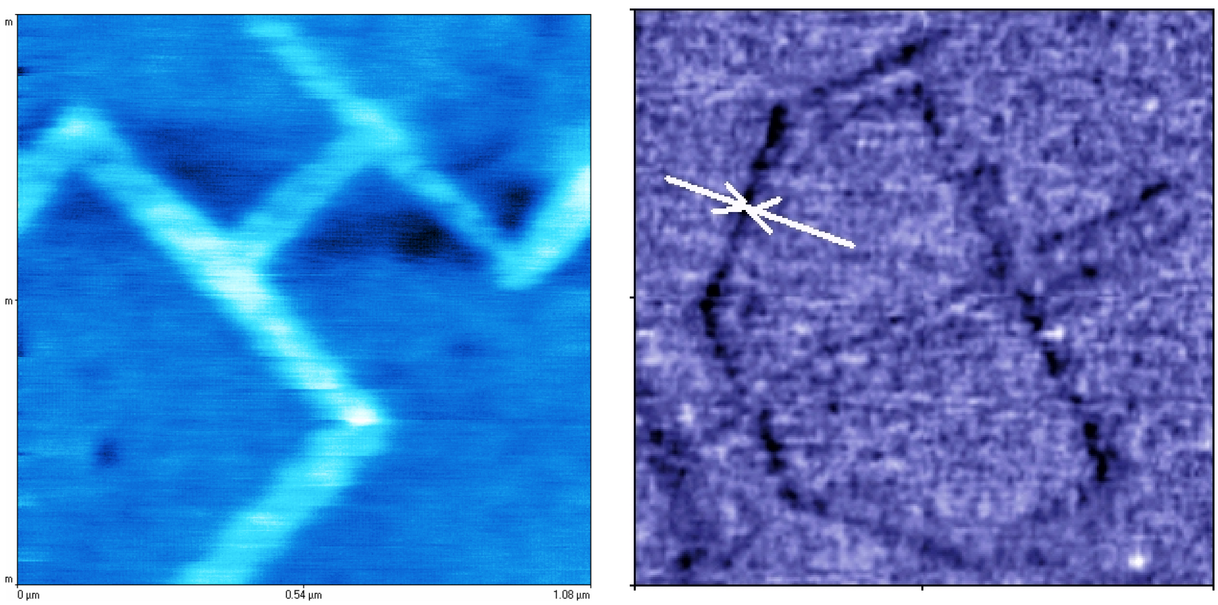

Figure 2: (a) Topography scan used for height measurement; (b) LFM scan and line width measurement. Scan sizes are 1 µm.

From these oxidation experiments, we found that the maximum height of grown oxide was 5 nm, as measured from data displayed in Figure 2a. The narrowest lines achieved were 30 nm, as measured from the lateral force image in Figure 2b. If produced on an ultra-thin titanium layer rather than silicon, these structures could act as barriers to electron transport through a narrow channel. A narrow enough channel could act as a tunnel barrier, as indicated in Figure 2b. In summary, the bias control option of the NSCRIPTOR System is easily integrated as an additional experimental parameter for making nanoscale patterns.

For more information including pricing, please contact NanoInk Sales Department at sales@nanoink.net or 1-847-679-NANO.

Bibliography

1) Y. Li, B.W. Maynor, J. Liu. Electrochemical AFM "Dip-Pen" Nanolithography. *J. Am. Chem. Soc.*; **123**; pp. 2105-2106; 2001.
2) S. F. Lyuksyutov, R. A. Vaia, P. B. Paramonov, S. Juhl, L. Waterhouse, R. M. Ralich, G. Sigalov, E. Sancaktar. Electrostatic nanolithography in polymers using atomic force microscopy. *Nature Mat.*; **2**; pp.468-472; 2003.
3) B. Irmer, K. Kehrle, H. Lorenz, J. P. Kotthaus. Nanolithography by non-contact AFM-induced local oxidation: fabrication of tunneling barriers suitable for single-electron devices. *Semicond. Sci. Tech.*; **13**; pp. A79-A82; 1998.
4) P. Avouris, R. Martel, T. Hertel, R. Sandstrom. AFM-tip-induced and current-induced local oxidation of silicon and metals. *Appl. Phys. A*; **66**; pp. S659-S667; 1998.
5) M. Calleja, R. Garcia. Nano-oxidation of silicon surfaces by noncontact atomic-force microscopy: Size dependence on voltage and pulse duration. *Appl. Phys. Lett.*; **76**; pp. 3427-3429; 2000.